The Virtex-5 Routing and Logic Architecture

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Abstract – This report presents the architecture of Xilinx Virtex-5 – the first FPGA device fabricated at the at the 65 nm technology node. Switching from 90 nm to 65 nm enables a better output, higher density (the number of LEs in a single chip) and reduced energy consumption. Meanwhile, due to the increased logic density and the conducting architecture inherited from the previous preceding Virtex-4 generation of devices, the necessary overall length of the connecting wires is now considerably greater. Hence, there is a need of an improved connecting architecture for routing.

Keywords – **FPGA, FPGA Architecture, Routing, Logic Block**

I. INTRODUCTION

The architecture of the modern SRAM-based FPGA devices comprises logic blocks (LB) symmetrically organized in a matrix of rows and columns, with routing channels round it. These channels contain a certain number of programmable links, interconnecting the logic blocks (fig.1).

The input/outputs (I/Os), connecting FPGA blocks to external devices, are located in the architecture's periphery.
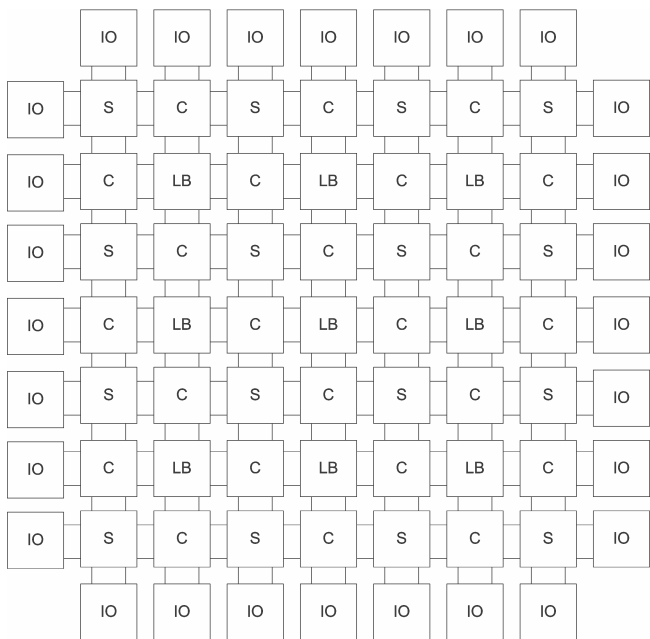

Fig. 1. FPGA architecture of matrix structure

A. Logical blocks architecture

Logic blocks (LB) comprise a number of base logical elements (BLE), forming a single logical group (fig.2).

'*I*' marks the number of inputs within the logical group, while the outputs are equal in numbers to the BLEs, i.e. *N*.

Each BLE features a single LUT element with K inputs and a D-trigger. The LUT element is a logic structure that enables the realization of any logic function with K number of variables.

It is with the 2-input multiplier that one opts between taking the BLE output from the D-trigger or not (fig.2 (a)).

Each logic group is 'completely interconnected, which means each I-input and each N-output could be linked to any K-input of the LUT element. For this purpose, multipliers connected to the BLE inputs are used, as indicated on fig. 2 (b).

The number of inputs in the logic group is specified according to (1). This provides for the complete BLE usage in the group. (3)

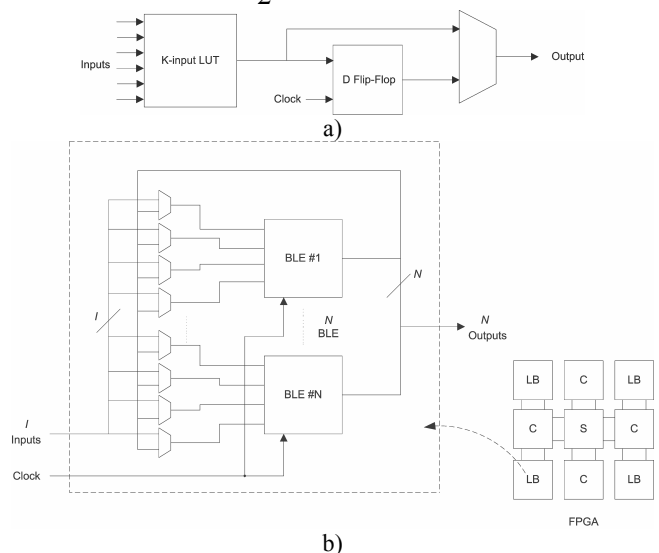$$I = \frac{K}{2}(N+1) \tag{1}$$

Fig. 2. BLE structure (a) and a logic group (b).

The input/outputs (I/Os) pad of a logic group can be situated in two, three or all planes of its four sides (fig.3).
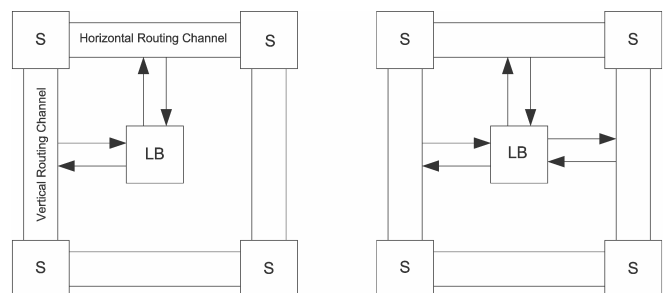

Fig. 3. Input/outputs pad of the logic group

B. Architecture of the routing channels

In the FPGA schemes of matrix structure, in-between the LB rows and columns, there are horizontal and vertical routing channels, of which the length equals the number of LB in a single row or column. The part of the channel that is adjacent to the LB is called channel segment. Each channel segment consists of W number of links/wires. Here, W is the channel width.

In most FPGA schemes nowadays, all channel segments are equal in width. A conclusion is drawn in [3] that using different channel segment width results in minor improvements.

Likewise, in almost all FPGA schemes today, the routing channel architecture is unidirectional and each link within the channel is guided by a single source, subsequently chosen by a multiplier and a buffer (fig.4).
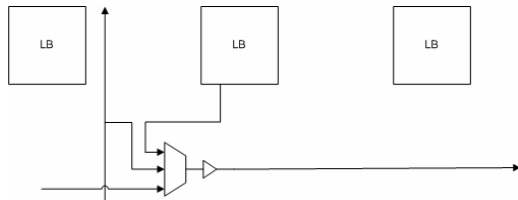The buffer output also marks the starting point of a given wire within the channel segment.

Fig. 4. FPGA with one-way architecture of the routing channels

In the case of the Xilinx' FPGA devices, these wires are denoted as 'unidirectional'.
'L' marks the wire length and it equals the number of LBs surrounding the wire. Fig.4 shows a wire with L=2.
There are experiments [X, Y, Z], proving that the best surface - delays ratio in the FPGA device can be attained by using wires with length of 4 and 8.
In the case of commercial architectures like Xilinx Virtex 4, 66% of the wires have L=6, 22% have L=2 and 13% have L=24, which is the horizontal and the vertical length of the entire chip.

This report presents the distribution of the wires with different length in the horizontal and vertical channels of Xilinx Virtex-5. To track down the wire distribution, the FPGA Editor – part of the Xilinx ISE 10.1i development environment – is put in practice.
The channel segment interconnection (vertical and horizontal) is performed by commutation blocks (marked S on fig.1).
A wire with channel segment neighboring S could be linked to a wire in any of the remaining and neighboring S segments through programmable switches, guided by multiplexers.
The flexibility (the extent of interconnectivity) of the commutation block is defined by the number of output wires, to which a single input wire could be linked.
 The connection between logic blocks (LB) and routing segments is enabled by connecting blocks (C). These connecting blocks enable two types of connections – between the LB input exits and channel segment wires and between LB output exits and channel segment wires. Thus,

two types of connecting blocks are formed – input and output.

II. Routing Architecture

A. Logic Block Architecture

The logic blocks in Virtex-5, bearing the Xilinx notion 'configurable logic blocks (CLBs), consist of two elements called 'slices' (fig.5), and each 'slice' features four LUT elements with 6 outputs each (fig.6).

Table 1 contains the general differences in the logic architecture of Virtex-4 and Virtex-5.
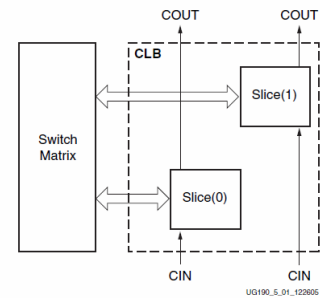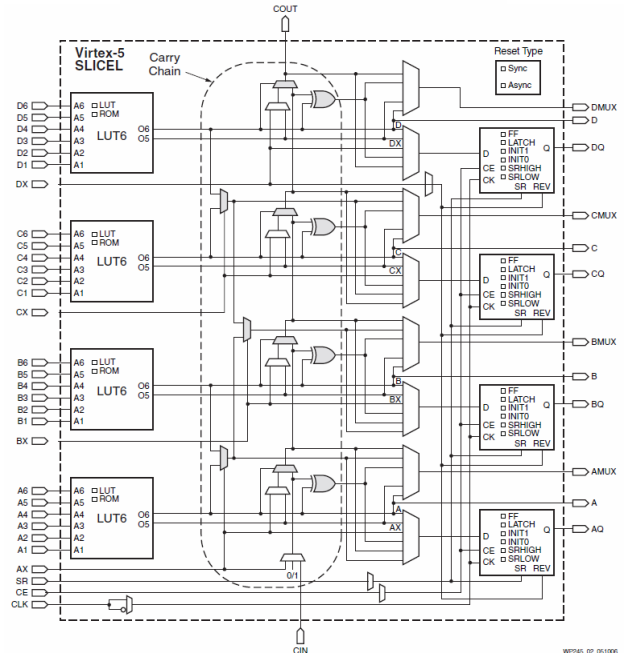

Figure 5-1: Arrangement of Slices within the CLB

Фиг. 6. Structure of the slice element within Virtex-5.

Table 1. Comparison between the logic architectures of Virtex-4 and Virtex-5

CLB	Virtex-4 FPGA	Virtex-5 FPGA
Slices	4	2
LUTs	8	8
Flip-Flops	8	8
Clocks, Clock-Enables, Reset	4 each	2 each
Distributed RAM	64 bits	256 bits

Shift Register Length	64 bits	128 bits
Multiplexers	16 – 1	2 x (16 – 1)

Proofs of the advantages of using 6-input LUT elements are given in [A]. The main reason for replacing the 4-input LUT elements, used in the previous generations of FPGA Viretx chips, with 6-input ones is the improved ratio between the delays in the schemes and the utilized surface in the case of the 65 nm technology node (fig.8) [B].
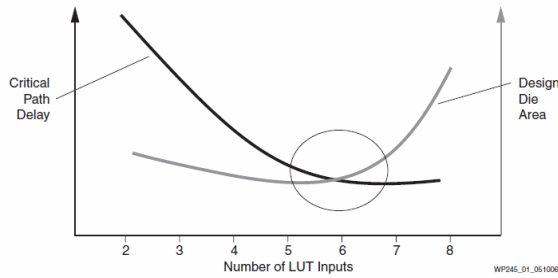

Figure 1: **Making the Right Trade-off for LUT Input Architecture at 65 nm**

B. Modification to Routing Architecture

Compared to its Virtex predecessors, the wiring architecture in Virtex-5 has been considerably modified (fig. 8). This is a result of the increased logic density and the imperfections of the traditional connecting architecture.

There is a dependency between the number of logic components in a single LB and the necessary quantity links to the other LBs in a single chip. This dependency is also known as the principle of Rent [C]:

$$T = t \cdot C^p \qquad (2)$$

Where *T* marks the number of terminals (or the outputs on the four sides of the logic block), *C* is the number of the LB's internal components, *t* (the Rent constant) indicates the average number of terminals in a single logic block and *p* (Rent exponent – constant between 0 and 1) characterizes the logic complexity implied in the logic block. Generally, *p* ranges from 0.5 up to 0.75 for the most complex logic structures.

Table 1 is indicative of the equal number of LUT elements and triggers within a single logic block in Virtex-4 and Virtex-5. The difference hides in the number of LUT element inputs, which are 50% more in the case of Virtex-5. The way LUT elements are constructed implies that 50% more logic is needed for realizing 6-input LUTs, compared to the 4-input LUTs.

Taking this into account and applying the principle of Rent (2), it can be calculated that the necessary quantity of links within LB in Virtex-5 is 50% higher, provided that the traditional wiring structure of Virtex-4 remains in place. In order to evade such a surge in the number of routing wires, hence an increase in both the delays and the utilized surface, Virtex-5 uses an improved version of the wiring architecture named 'Diagonally symmetric interconnect pattern' (fig. 8). This type of architecture reduces the delays, thus making more LBs accessible with a smaller number of 'hops' (switch blocks). A 'hop' is created every

time a single wiring segment is used for setting up a link between two logic blocks (CLBs), be they neighboring or not. If two different segments are needed to set up a link between two logic blocks, then we have 2 'hops'. Table 2 displays the number of logic blocks, accessible with 1, 2, and 3 'hops' from a central CLB.
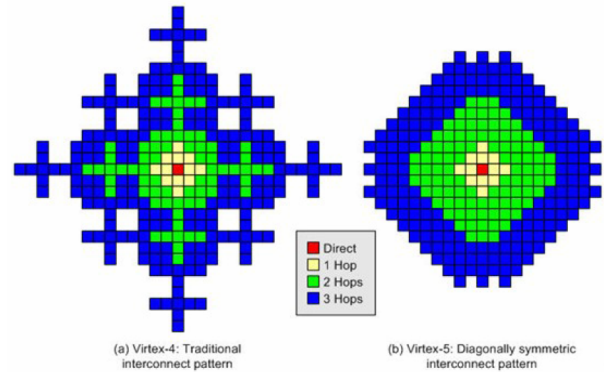

Figure 3: Interconnect Pattern for Virtex-4 and Virtex-5

With the process of IS constantly improving and the width of the MOS transistor channels constantly narrowing, the number of delays in the logic elements has been brought down at the expense of increased time lags in the connecting wires, or over 50% of the schemes' total delays. That's why it expedient to reduce the distances separating the logic blocks by raising the number of blocks reachable by 2 and 3 'hops'.

Figure 9 shows a comparison between the delays in the wiring architectures of Virtex-4 and Virtex-5 [P].
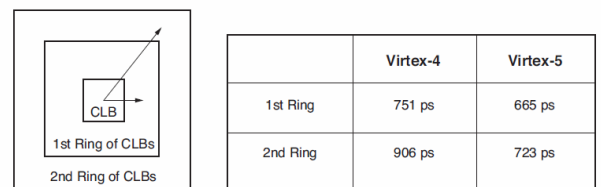

		Virtex-4	Virtex-5
1st Ring		751 ps	665 ps
2nd Ring		906 ps	723 ps

Figure 4: **Routing Delay Comparison for Virtex-4 and Virtex-5 FPGAs**

TABLE 2. COMPARISON BETWEEN THE ROUTING RESOURCES OF VIRTEX-4 AND VIRTEX-5

Hops	Number of CLB Reachable	
	Virtex-4 FPGA	Virtex-5 FPGA
1	12	12
2	68	96
3	200	180
Total	280	288

To implement the new diagonally-symmetrical architecture, instead of using the traditional segments of lengths double (covering 2 logic blocks), hex (covering 6 logic blocks) and long (covering all logic blocks in a single row or a column), segments of lengths double (2), pent (5) and long are used.

To enhance the architecture flexibility, some of the segments of length are shaped in the mould of the letter G, which means that part of the segment covers 3 or 4 LBs in a horizontal channel, while another part of it covers 1 or 2 LBs in a vertical channel. This is a proper way of detouring the limitations in the utilized double-sided routing architecture of Virtex, whereby the LB could connect to all wires in a horizontal and a vertical channel (the links are with half of the wires above and the other half below LB) (fig.3).

Table 3 displays the generalized differences in the routing segments between Virtex-4 and Virtex-5. The results shown in the table have been obtained in a survey performed with the FPGA Editor program, which is part of the integrated software environment Xilinx ISE 10.1i (fig.10).

necessary links inside the chip and a greater overall length of the wires.

To resolve this problem, Xilinx used a different to the Virtex-4 routing architecture, comprised of wires of length 5, part of which are in the form of the letter G.

Thus, the distance between the LBs is shortened and the number of CLBs reachable with 2 and 3 'hops' is on the rise. This is a way of not only boosting the speed, but of reducing the amount of energy consumed, too, as it takes smaller amounts of energy for transiting the signal down the metallic sections in the given IS layer and travel the distance from one block to another.

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Фиг. 10. Screenshot of FPGA Editor.

TABLE 3. COMPARISON BETWEEN THE ROUTING RESOURCES OF VIRTEX-4 AND VIRTEX-5

Wire segments in channel	Virtex-4 FPGA	Virtex-5 FPGA
Double (length 2)	40	42
Hex (length 6)	120	-
Pent (length 5)	-	120
Long (length long)	24	18
Total	184	180

III. Conclusion

This paper presents the architecture of the modern SRAM-based FPGA devices. It focuses on the architectural specifications of the FPGA generation of Xilinx Virtex-5 devices. Virtex-5 is the latest generation of devices of producer Xilinx. Here the specifications of Virtex-5 are reviewed and their option is grounded.

Compared to its predecessor Virtex-4, Virtex-5 uses 6-input LUT in combination with an enhanced routing architecture and a shift from the 90 nm to 65 nm technology node. Thus, their output is 30% higher.

The shift to a technology node with a smaller channel width of the comprising transistors means higher density and a rise in the number of logic elements inbuilt in the chip. Thus, according to the principle of Rent, means more

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